the Examiner reconsider the rejection of the claims in view of the amendments and comments set forth below.

CLAIMS

Please amend the claims as follows:

1. (amended) A semiconductor device comprising:

a substrate;

a row of transistors disposed on the substrate, each transistor having a stacked gate structure and a drain, wherein adjacent transistors are isolated from each other by P-type regions of the substrate;

fig. 2-5

a layer of ~~type-2~~ polysilicon interconnecting the transistors in the row; and

a source region comprising an N-type region of the substrate adjacent to the row of transistors ~~layer of type-2 polysilicon~~ and having a contact coupled thereto, wherein the ~~and a~~ N-type ~~junction~~ region includes a plurality of P-type regions that have been over-doped to form N-type regions, and wherein [the] an N-type junction extends ~~extending~~ across the source region to provide ~~that provides~~ a planar electrical path between the drains of the transistors and the contact, thereby reducing resistance of the source region.

10

A1

2. (amended) The semiconductor of claim 1 wherein the transistors are located in core regions of the substrate ~~and isolation regions between pairs of adjacent transistors comprise respective P-type regions~~.

3. (original) The semiconductor of claim 1 wherein the transistors are located over active areas in the substrate, and the active areas include N-type regions.

4 - 10. (withdrawn 12/19/2002)

11. (new) A semiconductor device comprising:

Contd A1

a stacked gate structure;

a first p-type region of substrate disposed adjacent to a first side of the stacked gate structure;

fig. 2-5

a first n-type region of substrate disposed adjacent to a second side of the stacked gate structure; and

a second n-type region of substrate disposed adjacent to the first and second regions, the second n-type region including p-type dopants at a concentration corresponding to the first p-type region.

1, 8

12. (new) The semiconductor device of claim 11, wherein the second n-type region further comprises n-type dopants at a concentration sufficient to over compensate for the p-type dopants.

1, 8

13. (new) The semiconductor device of claim 11, wherein the stacked gate structure is located in a core portion of an integrated circuit device.

14. (new) The semiconductor device of claim 11, wherein the stacked gate structure, p-type region, and the first and second n-type regions form a memory cell, and the semiconductor device comprises a plurality of the memory cells.

Cntd A1

15. (new) The semiconductor device of claim 14, wherein the memory cells are organized into rows and columns.

16. (new) The semiconductor device of claim 15, wherein the p-type [regions] (region) are disposed between memory cells within a row and the first n-type [regions are] (region is) disposed between memory cells within a column.

17. (new) The semiconductor device of claim 11 further comprising:

a second p-type region of substrate disposed adjacent to a third side of the stacked gate structure, the third side being opposite the first side;

a third n-type region of substrate disposed adjacent to a [forth] (fourth) side of the stacked gate structure, the [forth] side being opposite the second side; and

[a [forth] (fourth) n-type region of substrate disposed adjacent to the third and [forth] regions, the forth n-type region including p-type dopants at a concentration corresponding to the second p-type region.

18. (new) The semiconductor device of claim 17, wherein the [forth] n-type region further comprises n-type dopants at a concentration sufficient to over compensate for the p-type dopants.

19. (new) The semiconductor device of claim 17 further comprising:

112 1st 2 [a fifth n-type region of substrate disposed adjacent to the first and [forth] regions, and

Cancel A1

a sixth n-type region of substrate disposed adjacent to the second and third regions, the fifth and sixth n-type regions including p-type dopants at a concentration corresponding to the first and second p-type regions.]

20. (new) A semiconductor memory comprising:

a plurality of stacked gate memory cells disposed on a substrate and organized into rows and columns;

a plurality of p-type regions of substrate disposed between adjacent memory cells within a row of memory cells;

a plurality of n-type regions of substrate disposed between adjacent memory cells within a column of memory cells; and

[a plurality of compensated n-type regions of substrate disposed between the p-type

112 1st regions, the compensated n-type regions including a p-type dopant at a first predetermined concentration.]

21. (new) The semiconductor memory of claim 20, wherein the compensated n-type regions of substrate include an n-type dopant at a concentration sufficient to over compensate for the p-type dopant.

22. (new) The semiconductor memory of claim 20, wherein the plurality of stacked gate structures are located in a core portion of the semiconductor memory.

23. (new) The semiconductor memory of claim 20, wherein the plurality of n-type regions and the plurality of compensated n-type regions form a source region for each row of memory cells.

24. (new) The semiconductor memory of claim 23, where in [each] source region comprises alternating n-type regions and compensated n-type regions.

25. (new) The semiconductor memory of claim 24 further comprising [a plurality of electrical contacts, each electrical contact coupled to a corresponding one of [the plurality of source regions].